1. A tilt-angle implant method of forming an LDD (Lightly Doped Drain) in a high voltage device comprising the steps of:

providing a silicon substrate having a plurality of active and field regions defined;

forming a thick gate oxide layer over said substrate;

forming a gate electrode over said thick gate oxide layer;

performing a first ion implantation with a tilt-angle;

forming oxide spacers on sidewalls of said gate electrode; and

performing a second ion implantation with no tilt-angle.

2. The method of claim 1, wherein said forming said thick gate oxide layer is accomplished by chemical vapor deposition at a temperature between about 450 to 600°C.

3. The method of claim 1, wherein said gate oxide layer has a thickness between about 3000 to 5000 angstroms (Å).

4. The method of claim 1, wherein said forming said gate electrode is accomplished by depositing a polysilicon layer at a temperature between about 570 to 625°C, and patterning said polysilicon layer.

5. The method of claim 4, wherein said patterning said polysilicon layer is accomplished with an etch recipe having gases Cl_2 and HBr.

6. The method of claim 4, wherein said polysilicon layer has a thickness between about 1000 to 2000 Å.

7. The method of claim 1, wherein said performing said first ion implantation for an NMOS device is accomplished with phosphorous ions at a dosage level between about $1x10^{13}$ to $5x10^{13}$ atoms/cm^2, and at energy level between about 35 to 55 KeV.

8. The method of claim 1, wherein said tilt-angle is between about 40 to 45 degrees.

9. The method of claim 1, wherein said performing said first ion implantation for a PMOS device is accomplished with boron ions at a dosage level between about $1x10^{13}$ to

$5x10^{13}$ atoms/cm^2, and at energy level between about 20 to 35 KeV.

10. The method of claim 1, wherein said performing said first ion implantation is accomplished by rotating said substrate at a tilt-angle between about 40 to 45°.

11. The method of claim 1, wherein said forming said oxide spacers on sidewalls of said gate electrode is accomplished by depositing an oxide layer to a thickness between about 1200 to 1500 Å, and then anisotropically etching said oxide layer.

12. The method of claim 1, wherein said performing said drain ion implantation is accomplished with As ions at a dosage level between about $2x10^{15}$ to $5x10^{15}$ atoms/cm^2, and at energy level between about 40 to 60 KeV.

13. An optimum implant angle method of forming a DDD (Doubly Doped Drain) in a stacked flash memory cell comprising the steps of:

providing a silicon substrate having a plurality of active and field regions defined;

forming a gate oxide layer over said substrate;

forming a floating gate over said thick gate oxide layer;

forming an inter-gate oxide layer over said floating gate;

forming a stacked control gate over said inter-gate oxide;

forming oxide spacers on sidewalls of said stacked gate;

performing a first lightly doped implantation with an optimum tilt-angle; and

performing a second heavily doped implantation with an optimum tilt-angle.

14. The method of claim 13, wherein said gate oxide layer has a thickness between about 80 to 95 Å.

15. The method of claim 13, wherein said forming said floating gate is accomplished by depositing a first polysilicon layer to a thickness between about 1000 to 2000 Å, and then etching said first polysilicon layer.

performing a drive-in diffusion of said doubly doped drain, DDD.

24. The method of claim 23, wherein said plurality of gates are floating gate and control gate of said flash memory cell.

25. The method of claim 23, wherein said optimum angle is between about 40 to 50 °.

26. The method of claim 23, wherein said performing said first lightly doped implantation is accomplished with phosphorous ions at a dosage level between about $1x10^{13}$ to $5x10^{13}$ atoms/cm^2, and at energy level between about 35 to 55 KeV.

27. The method of claim 23, wherein said performing said second heavily doped implantation is accomplished with arsenic ions at a dosage level between about $2x10^{15}$ to $5x10^{15}$ atoms/cm^2 at energy level between about 40 to 60 KeV.

28. The method of claim 23, wherein said performing said drive-in diffusion of said DDD is accomplished at a temperature between about 850 to 950°C.

29. A stacked gate having a doubly diffused drain (DDD) comprising:

a junction having a lightly doped profile; and

a surface region having a heavily doped profile.

30. A stacked gate of claim 29, wherein said lightly doped profile comprises phosphorous ions at a dosage level between about $1x10^{13}$ to $5x10^{13}$ atoms/cm^2.

31. A stacked gate of claim 29, wherein said heavily doped profile comprises arsenic ions at a dosage level between about $1x10^{15}$ to $5x10^{15}$ atoms/cm^2.